

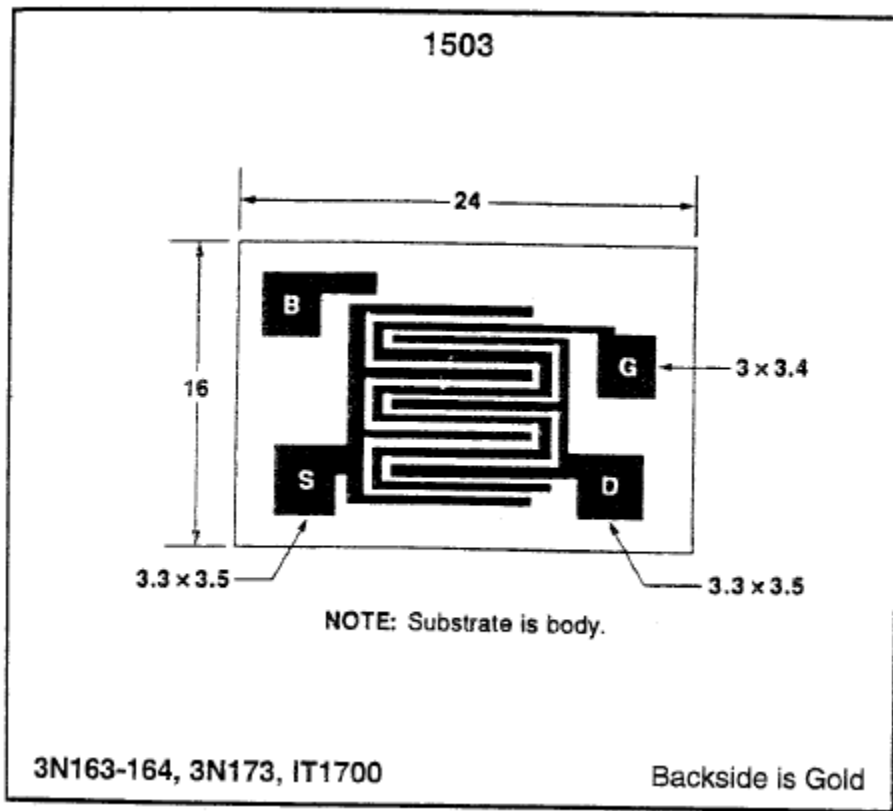


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material:**  
**Backside Material: Au**  
**Bond Pad Size:**  
**Backside Potential:**  
**Mask Ref:**

**APPROVED BY:DK**

**DIE SIZE: .024 x .016**

**DATE: 6/29/10**

**MFG: Calogic**

**THICKNESS:**

**P/N:3N172**